A Multi Gigabit Clock and Data Recovery Testchip fabricated in 0.18\textmu m CMOS

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Introduction

• In standard SerDes system, each transceiver has its own local reference clock.
• If clock is distributed through serial data port, clock and data recovery (CDR) circuit has to operate without local reference clock.
• The recovered clock must have sufficient jitter performance to be used as reference clock for local components such as ADC or serializer.
• The conventional half-rate-clock CDR using ring-based oscillator, as using in OASE, do not have sufficient jitter performance.
• Therefore, the feasibilities of low jitter CDR using LC-based oscillator and the improved 1/4th-rate-clock CDR using ring-based oscillator are investigated.
Clock Data Recovery (CDR) Testchip
Technology : UMC 0.18 µm CMOS with RF options
Chip Area : 1525 µm x 4960 µm

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Test structure CDR-1 “CDR full-rate Quadricorrelator FD Structure”

- CDR can operate without local reference clock.
- Quadricorrelator frequency detector can provides information of frequency difference between VCO clock and serial data steam.
- CDR with FD can have low loop bandwidth and wide pull-in range.
**Principle of quadricorrelator frequency detector**

- consists of 2 sets of phase detector with different clock phases
- Q1 and Q2 show the frequency difference.
- Phase difference of Q1 and Q2 shows the sign of frequency difference.

Ex. If $\Delta \omega$ is positive Q1 leads Q2

If $\Delta \omega$ is negative Q2 leads Q1 because $\sin(-\Delta \omega t) = -\sin(\Delta \omega t)$

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**Diagram**

- Serial Data In
- $\cos(\omega_{\text{clk}} t)$
- $\cos(\omega_{\text{data}} t)$
- $90^\circ$ Delay
- $\sin(\omega_{\text{clk}} t)$
- $\cos(\omega_{\text{clk}} t)$
- $\sin(\omega_{\text{data}} t)$

**Frequency-locked loop**

- VCO
- LPF
- PD
- LPF
- LPF
- LPF
- PD

$\Delta \omega = \omega_{\text{clk}} - \omega_{\text{data}}$

PD : Phase Detector
LPF : Low-passed Filter
CDR using digital quadricorrelator frequency detector

Serial Data In

Clk 0° (full rate)

D-FF (CML)

D-FF (CML)

D-FF (CML)

D-FF (CML)

D-FF (CML)

Control logic (CMOS)

Charge Pumps & Loop Filter

Quadrate phase LC-VCO

Recovered Data

Freq. Up

Freq. Down

Phase Up

Phase Down

DET FF : Double-edge-triggered Flipflop
PFD Logic of CDR-1: F-VCO too low

- Both edges of serial data sampling clk-0 and clk-90 to generate Q1 and Q2.
- Q1 and Q2 are used to generate F-Up, F-Down, P-Up and P-Down.
Measurement results: CDR-1

a) Incoming serial data in, 2.5 Gbps, PRBS 2^7-1

b) Jitter histogram of the recovered clock, 2.5 GHz., jitter 2.3 ps, rms

c) Incoming serial data in, 2.5 Gbps, jitter 280 ps, p-p (0.7UI) at 10MHz. modulation

d) Jitter histogram of the recovered clock, 2.5 GHz., jitter 5.9 ps, rms
Measurement results: CDR-1

- Technology: 0.18µm CMOS
- Active area:
  - CDR: 0.71 mm²
  - Loop Filter: 0.69 mm²
- Power consumption: 140 mW at 1.8 Vdd
- Data rate: 2.41 - 2.72 Gbps
- Loop bandwidth: 1.3 MHz.
- Pull-in range: > 100 MHz.
- Jitter Performance
  - Input Data
    - 2.5 Gbps, PRBS 2⁷-1: 2.3 ps, rms
    - 2.5 Gbps, jitter 280 ps, p-p: 5.9 ps, rms
  - (0.7UI), modulation at 10 MHz.

Die Photograph

Recovered clock, 2.5 GHz.
Test structure CDR-3 “CDR using 1/4\textsuperscript{th}-rate Quadricorrelator FD Structure”

```
phase offset compensation
clk-0 – clk-15
8-phase ring oscillator VCO
CP & Loop filter
PFD logic
Recovered & 1:4 demultiplexed Data
Serial Data In
Sense-amp x 16
Sampling Data
```

Serial Data In
8-phase clock

UI

(clock period = 4 UI)

(a)(b)(c)

Clk. too early

(t)

Clk. too late

(t)
- F-VCO > Data rate /4, data transitions rotate from case-1 -> case-2 -> case-3 -> case-4.
- F-VCO < Data rate /4, data transitions rotate from case-1 -> case-4 -> case-3 -> case-2.
- In lock condition, clk-0 sampling at the middle of data-eye, edges of data are in case-2 or case-3.
  - PD generate “late” signal (f-up) for case-1 and case-2.
  - PD generate “early” signal (f-down) for case-3 and case-4.
1/4th-rate PFD Block Diagram

Sense-Amp x 16

Retiming

Edge Detectors

Edge Detectors

Edge Detection Logic

Late Case-1

Late Case-2

Early Case-3

Early Case-4

FD Logic

PD Logic

F-Up (case-1,2)

F-down

disable

F-up

disable

Gating

Gating

DEMUX

4-bit Output

Multi-phase clock from VCO

to Charge Pump

F-Down (case-3,4)
FD Logic of CDR-3: F-VCO too low

- clk0
- clk1
- clk2
- clk3
- clk4
- clk13
- clk14
- clk15

Case-4 (Q1-set)

Case-2 (Q1-reset)

Q1

Case-3 (Q2-reset)

Case-1 (Q2-set)

F-up disable

F-down disable

Rising-edge of Q1 & Q2 = 1

Falling-edge of Q1
**Measurement results: CDR-3**

- **a)** Incoming serial data in, jitter 6.6 ps, rms
- **b)** Corresponding recovered clock, jitter 7.9 ps, rms
- **c)** Incoming serial data in, jitter, p-p 311ps (0.7 UI) at 10MHz.
- **d)** Corresponding recovered clock, 15.7 ps, rms
Measurement results: CDR-3

- Technology: 0.18µm CMOS
- Active area:
  - CDR + DEMUX: 0.70 mm²
  - Loop Filter: 0.63 mm²
- Power consumption: 100 mW at 1.8 Vdd
- Data rate: 1 - 2.27 Gbps
- Loop bandwidth: 1MHz.
- Pull-in range: > 100 MHz.
- Jitter Performance:
  - Input Data: 2.25 Gbps, PRBS 2^7-1: 7.9 ps, rms
  - 2.25 Gbps, jitter 311 ps, p-p: 15.7 ps, rms (0.7UI), modulation at 10 MHz.

Deserialzer Outputs at 562.5 MHz. (2.25 Gbps)
Conclusions

• CDR with Frequency Detector
  - can operate without the need for a local reference clock.
  - low jitter operation and wide pull-in range can be achieved.
• Full-rate CDR architecture,
  - suitable for LC-VCO, very low jitter.
  - phase frequency detector is implemented in CML.
• 1/4th-rate CDR architecture,
  - lower operation frequency, suitable for ring-based oscillator.
  - all logic units can be implemented by CMOS logic, low power.
  - intrinsic 1- to - 4 DEMUX.
  - phase offsets of VCO can be reduced by layout techniques and skew calibration scheme.

• The tested CDRs implemented on 0.18μm CMOS Technology has low jitter operation.